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JUNE 2012
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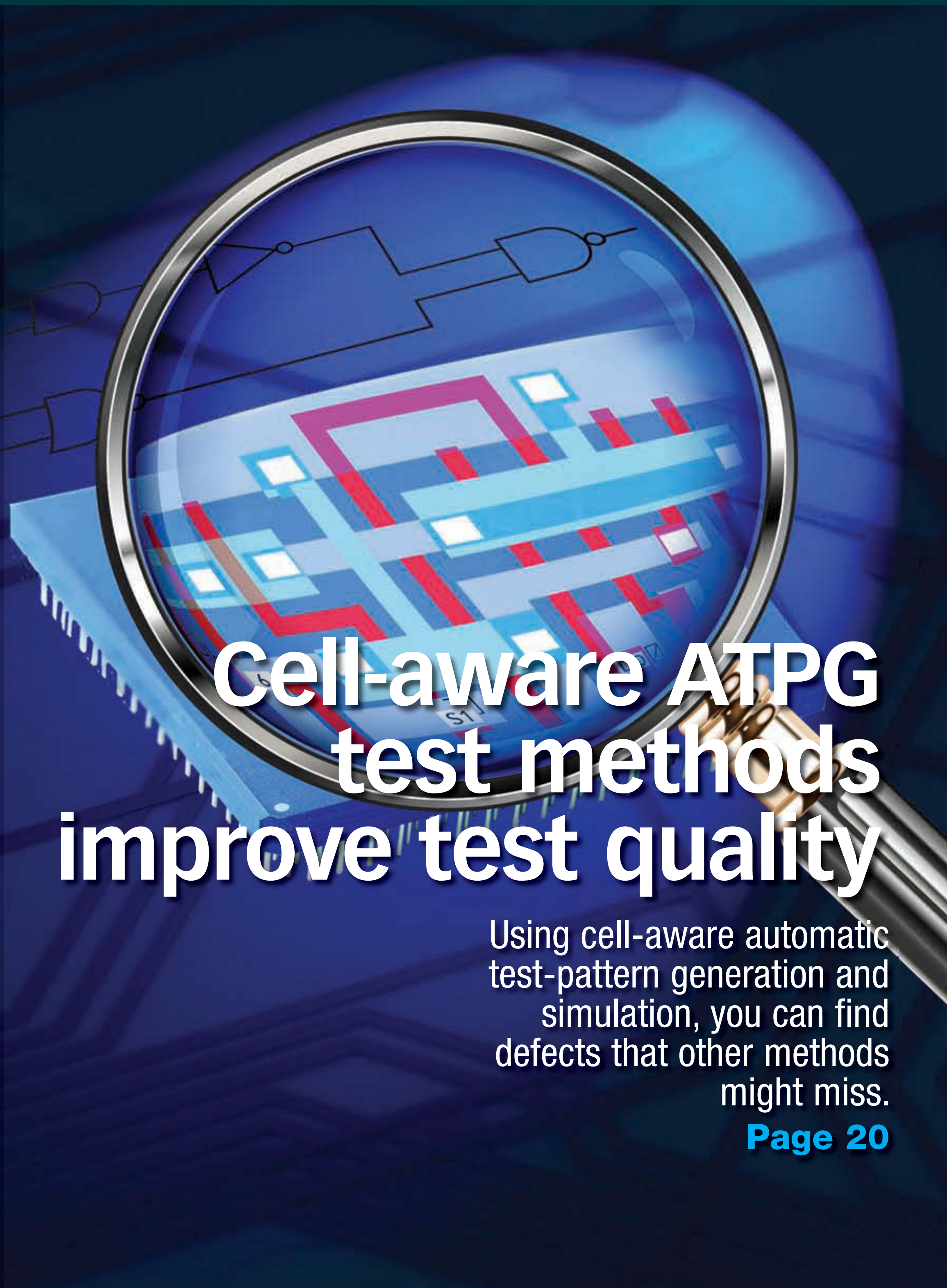
Test & Measurement World

THE MAGAZINE FOR QUALITY IN ELECTRONICS



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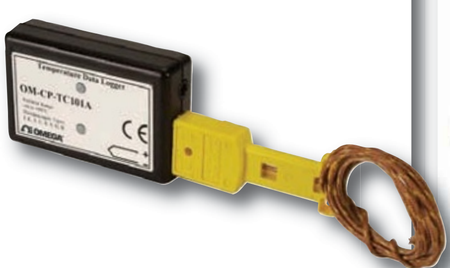

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A knobless world?

A couple of months ago, "Scope Junction" ran an informal survey on the preferred user interfaces for an oscilloscope. The majority responded with a preference for "old school" knob and button interfaces. This is not surprising, but is this a trend that will last?

bit.ly/IRYr19

How's my divining?

At the end of 2011, I made 10 predictions about the industry for 2012. I thought I'd review the predictions to see how I'm doing. It is also a good way to step back and take a look at the industry as a whole.

bit.ly/JsPWoQ

Precompliance testing for radiated emissions

One of the biggest frustrations for smaller companies is how to get a reasonable idea about whether a product will pass or fail radiated emissions testing prior to formal qualification testing.

bit.ly/JqV0iB

Testing op amps requires stable test loops

The fourth installment in the "basics of testing op amps" series by David R. Baum and Daryl Hiser of Texas Instruments covers compensation issues you must address when using the suggested test circuits.

bit.ly/KO6ayj

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Test & Measurement World

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Taking the measure of a new era

This June 17–22 marks the 60th anniversary of the IEEE MTT-S International Microwave Symposium (IMS2012), or as we old hats refer to it, MTT. This year, the show is being held in Montreal, Canada, and I must admit I am looking forward to that. It looks like a fantastic venue (and an opportunity to dust off my French).

My first MTT show was in 1995, and the show still had its roots firmly in the military/defense market. Many were whispering, though, about the promise of commercial applications and the growth of a new commercial application that was being referred to as "wireless." There was plenty of chuckling about how this was not a new term, as the first radio was called a "wireless," but nonetheless, there was a ray of hope in a challenged market. How far we've come!

If new techniques are what you're looking for, this issue of *T&MW* is a great resource for you.

Those of you who know me know that I am a bit of a history buff, so I've been looking into the history of the show. Yes, MTT is a fabulous place to see all the latest test and measurement equipment and software and learn about some of the newest techniques for speeding time-to-answer and for testing the latest protocols, but it is also a show with a rich history.

The first show, simply called the Symposium on Microwave Circuitry, was held in 1952, and the first recipients of the "Annual Prize" were Nicholas Sakiotis and Herman Chait from the Naval Research Laboratory in Washington, DC, for their paper, "Properties of Ferrites in Waveguides." In 1961, the year the first digest was published, there were 20 papers presented at the show. This year, there promises to be more than 600.

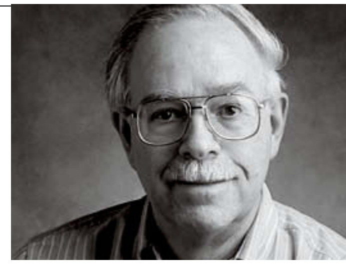
Of special note to those of us involved in test is a technical session on Wednesday, June 20, called "Unconventional Measurement Techniques" that will highlight research work being done for contactless measurements, on-wafer scattering-parameters measurements, chemical sensing, microwave impedance measurements, and a calibration technique for free-space applications. Engineers who want to know more about MIMO can attend a panel session on Thursday titled, "The Mathematics and Physics of MIMO." Also on Thursday, there will be a technical session called "Nonlinear Measurement Techniques" that promises to cover a range of topics from phase-noise measurements to intermodular-distortion phase analysis at high frequency.

On Friday, June 22, the 79th Automatic RF Techniques Group (ARFTG) Microwave Measurement Conference will also take place in Montreal. This year's theme is nonlinear measurements, and the technical program looks packed.

If new test techniques are what you are looking for, then in addition to what's on offer at IMS2012 and ARFTG, this issue of *Test & Measurement World* is a great resource for you. Our cover story from Ron Press at Mentor Graphics offers a cell-aware automatic test-pattern-generation method that aims to define and target faults within an IC's gates. For those of you working in wireless, Aeroflex's Robin Irwin has provided an article reviewing manufacturing test requirements for the IEEE 802.11ac WLAN standard. In addition, Surbhi Bansal and Sameer Saran from Freescale Semiconductor have done a nice job laying out a design-for-test technique for on-chip frequency measurements.

I hope you enjoy the issue. And I hope you make it to Montreal. If you see me there, please stop me and say, "Bonjour!" T&MW

BRAD THOMPSON
CONTRIBUTING TECHNICAL EDITOR
brad@tmworld.com



The tasteful test bench

In my May column ("5060-9436"), I briefly mentioned the inevitable demise of user-repairable test instruments due to age and the dwindling numbers of parts-donor instruments. Unfortunately, current-generation instruments include custom ICs (ASICs), and many manufacturers no longer offer service manuals or schematics. All this points to a future in which hardware hackers will find it increasingly difficult to equip a traditional test bench with used and repairable instruments at modest cost. So, what's next?

I'll speculate that in the not-too-distant future, an impoverished experimenter's test bench might resemble a kitchen counter replete with a collection of inexpensive purchased modules assembled and interconnected for the task at hand. In size and shape, these modules might fit into the flip-top tinned steel boxes that contain Altoids mints.

Amateur-radio practitioners and electronics hobbyists pioneered the practice of stuffing home-brewed electronics into mint tins, but a few manufacturers now offer products that rival the performance offered by many traditional test instruments and also fit comfortably in these small containers.

For example, Valon Technology's Model 5007 Dual Synthesizer (**photo**) delivers two independent RF outputs spanning 137.5 MHz to 4.4 GHz at selectable RF levels 7, 4, 1, –2 (+8 to 0 dBm). Measuring 2-by-2 in., the 5007 derives its control signals from a USB interface and vendor-supplied PC and Macintosh software. Drivers are available for Linux and National Instruments' LabView. At $29, the 5007 is an inexpensive solution to many requirements for dedicated RF signal sources.

And now for dessert: Based on a 700-MHz ARM processor and offered as an inexpensive teaching aid, the under-$40 Raspberry Pi computer from the Raspberry Pi Foundation runs a Linux operating system and is said to be capable of desktop-PC performance. Add a user interface and a USB connection to a test module, and a Raspberry Pi computer running Linux and open-source data-acquisition and control software could serve as the heart of a low-budget test system. (The Raspberry Pi is currently back-ordered, but other microcontrollers may serve as well.)

Bon appétit! T&MW

To read past Test Voices columns, go to www.tmworld.com/testvoices.

ELECTRONICS IN MINT TINS

Given cellphones' ubiquity, fitting an entire radio transceiver in one's pocket may seem old hat, but amateur radio projects also include SWR (standing-wave ratio) meters, antenna-impedance matching networks, and RF amplifiers in mint tins:

longlist.org/Altoids+Transceiver

This site describes a basic video-display and audio-frequency tester:

bit.ly/M41yne

Here's an audio amplifier module in a mint tin:

tangentsoft.net/audio/cmoy-tutorial

…and a Part 15 FM-broadcast test transmitter:

bit.ly/KVD4qK

WHAT ELSE FITS IN A MINT TIN?

Clever hands have packaged survival kits, Ouija boards, and miniature dioramas in mint tins:

pinterest.com/jonadair/altoids-tins

RASPBERRY PI NOTES

The Raspberry Pi computer's capabilities and modest price has sparked considerable interest:

www.raspberrypi.org

Can't wait for the Raspberry Pi? Check out the Menta, an Arduino-family microcontroller that fits into a mint tin:

bit.ly/J5t0KY

OTHER FRUIT

Although mint tins offer electrostatic and magnetic shielding, they're not as rigid or as easy to machine as die-cast enclosures, such as those offered by Pomona Electronics (incidentally, Pomona was the ancient Roman goddess of fruit trees):

bit.ly/Jjy0PL

NEWSBRIEFS

Extech introduces 2-in-1 insulation tester and multimeter

The new MG300 from Extech Instruments is a true-rms multimeter with a built-in insulation resistance tester. The instrument's wireless data streaming provides added safety to users, who can monitor real-time readings on a laptop or computer screen from up to 30 ft away.

By adding insulation-testing capabilities to a DMM (digital multimeter), Extech has made it easier for electricians to make insulation testing a more routine part of predictive maintenance. The waterproof combination meter includes a digital insulation-resistance tester (or megohmmeter) with four test voltages for measuring resistance up to 4 GΩ with 0.001-MΩ resolution. The full-function DMM includes duty-cycle measurements and milliamp readings for analog 4–20-mA current loops in industrial analog process controls.

The MG300 meter includes a remote USB receiver and Windows-compatible software and is available with NIST-traceable certification. For users outside North America, Extech has introduced the MG302, which transmits data at 433 MHz instead of 915 MHz. www.extech.com/mg300.

Frost honors Agilent

Market-research firm Frost & Sullivan has awarded Agilent Technologies with the 2011 Global Frost & Sullivan Award for Company of the Year. Frost presents this annual award to the company that "demonstrated superior entrepreneurial ability in its industry during the research period."

In announcing the 2011 award, Frost noted that Agilent has worked to be a market leader through its introduction of products in all segments of the oscilloscope market. Agilent introduced the Infiniium 90000 X-Series for the high-end segment and introduced the InfiniiVision 2000/3000 X-Series for the mainstream segment. Agilent also designed and developed the high-performance ASICs that are at the heart of its oscilloscopes. In addition, the company has adopted indirect distribution channels for its mainstream oscilloscopes product line, which has played a role in the company's growth.

"The introduction of highly innovative products, the breadth of its portfolio that enables the provision of application-specific solutions, and the move toward indirect distribution channels for its mainstream oscilloscopes are some of the key reasons for Agilent's success," said Frost & Sullivan Industry Director Jessy Cavazos. www.frost.com.

IEEE works on camera-phone image quality

Although different models of camera phones may offer identical image resolution, they can produce images of vastly different quality, and vendors and consumers lack standardized metrics for comparing handsets. To remedy this, the

Editors' CHOICE

Teseq kit helps users develop interference test pulses

Teseq has introduced a development kit that automotive technicians and engineers can use to design their own pulse networks. The kit combines Teseq's FLX 5510 development board with the company's NSG 5500 automotive EMC test system. Engineers and technicians working in automotive EMC laboratories can use the kit to design test pulses that meet specifications such as pulse impedance, peak voltage, pulse width, and pulse-width under load.

Compatible with all NSG 5500 systems, the FLX 5510 contains two DIY 5510 submodules, one with a fully functional example circuit and one with an empty circuit that's ready to use. Plugging the DIY submodule into the FLX 5510 lets users design a pulse network that meets a specific need.

Engineers can use the development kit for conducted immunity testing, engineering investigations, quality control, fault analysis, and weak-spot analysis. The FLX 5510 produces pulses with peak currents of 300 A, a maximum voltage of 660 V, and a maximum pulse width of 30 ms. A software wizard lets users design custom pulsed waveforms. The FLX 5510 also works within Teseq's AutoStar 5 immunity software.

Teseq, www.teseq.com.

IEEE (Institute of Electrical and Electronics Engineers) has created the IEEE P1858 working group to develop methods and metrics for measuring and testing CPIQ (camera-phone image quality). The goal of IEEE P1858 is to create a CPIQ rating system that consumers can use to identify the camera phones that best meet their needs.

The P1858 working group will base its efforts on work that has been initiated by the I3A (International Imaging Industry Association). The I3A spent five years developing a comprehensive set of image-quality metrics and testing methods for camera phones. The IEEE acquired the I3A's CPIQ program and other assets and hopes to define tools and test methods that will facilitate standards-based communication and comparison among carriers, handset manufacturers, and component vendors. standards.ieee.org.

Editors' CHOICE

EB radio channel emulator claims highest capacity

Elektrobit's new EB Propsim F32 radio channel emulator is designed for mobile broadband testing, including 2G/3G, 3GPP LTE, and LTE-Advanced technologies. The instrument offers 32 channels, which Elektrobit reports is up to eight times more than other emulation systems on the market. For users who do not yet require this many channels, the emulator is available in eight- and 16-channel versions that can be upgraded to 32 channels if necessary.

Like all EB Propsim emulators, the F32 is designed to replicate wireless environments such as fading, noise, and spatial channel conditions. The emulator addresses the test requirements of multi-antenna technologies, such as spatial multiplexing, beamforming, and spatial diversity, and it enables testing scenarios for multi-RAT and multiband as well as 3GPP Rel 10 and 11 carrier aggregation, CoMP, and Relaying. The EB Propsim F32 also includes a setup wizard and 24/7 automated testing features.

Elektrobit, www.elektrobit.com.

Market Trends

Calibration services market on the rise

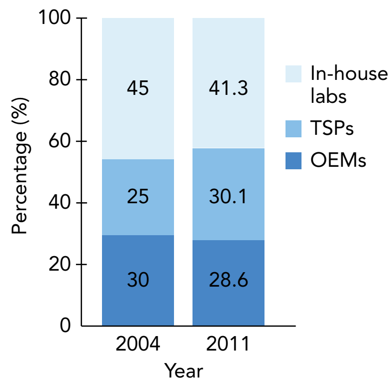
By Jessy Cavazos, Industry Director, Measurement & Instrumentation Practice, Frost & Sullivan

The total calibration services market in North America reached revenue of \$948.2 million in 2011. The market is expected to witness a compound annual growth rate of 5.4% from 2011 to 2018, although TSPs (third-party service providers) are expected to witness higher growth than OEMs (original equipment manufacturers) and in-house laboratories. By 2018, total revenue for the market is expected to reach \$1373.5 million.

Factors expected to have an impact on market growth include the stricter compliance environment and increased competition in key industries, which will increase the focus of customers on quality.

The growth in installed base of test and measurement equipment, as well as the increasing complexity of equipment, will also have a positive influence on the market. Suppliers of calibration services should beware, however, of the growth of modular instrumentation. Modular instrumentation has reached a significant share of the general-purpose test equipment market in North America, and customers can calibrate these instruments more easily than they could calibrate traditional instruments.

As the mix of products at customer locations has become more heterogeneous, the demand for calibration services for various types of equipment at one location is expected to further increase over the forecast period. Companies are striving to increase their capabilities



In the North American calibration services market, the percentage of revenue for TSPs has grown since 2004. (All figures are rounded.) Source: Frost & Sullivan

both organically and through partnerships and acquisitions. (*See the complete article at bit.ly/JhiJSJ.*)

LeCroy pushes RT DSO bandwidth war to 65 GHz, works on 100 GHz for 2013

By Dan Strassberg, Contributing Technical Editor

On April 24, only 13 days after Agilent Technologies had announced the availability of 63-GHz bandwidth in its Infiniium 90000Q RT DSO (real-time sampling digital-storage-oscilloscope) line, LeCroy revealed that its 10Zi series of LabMaster modular DSO systems would henceforth offer a 65-GHz bandwidth acquisition module. A mere two months earlier, LeCroy had brought forth the 10Zi line with an industry-leading maximum bandwidth of only 60 GHz.

The company ascribed its ability to offer the even-higher bandwidth to better-than-expected performance of the proprietary Si-Ge (Silicon-Germanium) ICs on which the 10Zi's operation depends. Perhaps even more significantly, LeCroy accompanied its announcement of the increased bandwidth with the news that it is working toward offering a 100-GHz bandwidth LabMaster acquisition module in 2013.

A 100-GHz LabMaster would not be LeCroy's first scope to achieve such bandwidth. It would, however, be its first (and presumably the industry's first) real-time DSO with such bandwidth. Approximately five years ago, LeCroy introduced the WaveExpert sequential-sampling-scope system, which offers 100-GHz bandwidth—but only for repetitive (albeit not necessarily periodic) signals.

In addition to what had been the only DSO bandwidths greater than 33 GHz, sequential-sampling instruments allow very high vertical resolution—typically 14 bits nominal, whereas ultrawideband RT DSOs generally offer only eight bits nominal. But because sequential-sampling DSOs usually require a new iteration of the input waveform for each data point they capture, measurements often take more than 1000 times as long as equivalent measurements with RT DSOs. The torpid pace of waveform acquisition therefore frequently frustrates signal-integrity engineers and electro-optical-communications-system designers who, until recently, had no alternative to the sequential-sampling instruments.

A LabMaster system that provides twenty 36-GHz-bandwidth channels or ten 65-GHz channels fits in a single "tower."

LeCroy may believe that it can get a 100-GHz RT DSO to market in less than 20 months because of its use of a proprietary frequency-domain-based architecture called DBI (digital bandwidth interleaving.) The company's two major competitors, Agilent and Tektronix, have historically relied upon a technology that can be called TDI (time-domain interleaving) or pipelining of ADCs. On paper, TDI is more straightforward than DBI, but implementing TDI in a system that must acquire a new sample approximately every 4 ps is anything but straightforward.

The beauty of DBI is that it divides a broadband signal into multiple frequency bands before simultaneously converting all bands from analog to digital and then merging the several streams into a single stream whose data rate is equal to the sum of the rates of the individual streams. The 65-GHz system uses two streams, each working with signals whose bandwidth is approximately 32.5 GHz—half of the input signal's 65-GHz-bandwidth. One signal is at baseband from the outset; the other is translated down to baseband before analog-to-digital conversion.

Each ADC converts at a rate of 80 Gsamples/s so there is no aliasing. The processes that merge the streams are not intuitive, but they result in a stream that, for the 65-GHz system, is indistinguishable from the stream you would create with pipelined converters operating at a combined rate of 160 Gsamples/s (see bit.ly/J9fMTK for LeCroy's explanation of the DBI process).

Extending the bandwidth to 100 GHz requires three streams, each with approximately the same bandwidth as that of each of the 65-GHz system's two streams. The effective conversion rate for the 100-GHz system is thus 240 Gsamples/s. An advantage of some three-stream DBI systems is that, without interleaving, the hardware modularity is based on four-channel groups. Three of those channels join to produce one maximum-bandwidth (in this case, 100-GHz) channel. Sometimes, it is possible to provide user access to the fourth channel, which, in this case, could process signals having 36 GHz bandwidth.

LeCroy says that it is still too early to predict whether its 100-GHz system will offer users a 36-GHz channel side-by-side with each 100-GHz channel, but because the LabMaster system accommodates as many as 20 acquisition modules, the company expects to be able to offer systems that users can configure for eighty 36-GHz channels, forty 65-GHz channels, or twenty 100-GHz channels. Such high channel counts are especially useful in work on multilane optical-communications systems.

Prices: LabMaster 10-65 acquisition module (65 GHz on two channels, 36 GHz on four)—$355,000; LabMaster 10-60 acquisition module (60 GHz on two channels, 36 GHz on four)—$315,000; LabMaster MCM-Zi master control module—$96,900. A working system requires one MCM and at least one acquisition module. *LeCroy, www.lecroy.com.*

PRODUCT TRYOUT

The incredible shrinking $199 DSO

I recently purchased a small digitizing oscilloscope, the "DSO Quad," from Seeed Studio. While this instrument may seem to merit consideration as a toy or, at best, a conversation piece, some of the specs are certainly worthy of the $199 price. I'm impressed that the entire product, plus the rechargeable LiPo (lithium polymer) battery, fits into such a small package.

The unit, which is slightly larger than a standard business card, comes with two Mueller 10:1, 100-MHz probes with tiny MCX RF coax connectors. The DSO Quad has two analog channels and two digital channels. The sampling rate is 72 Msamples/s. I measured a bandwidth of about 3 MHz.

The vertical scale is adjustable from 20 mV/div to 10 V/div (8-bit resolution), and the horizontal sensitivity is 0.1 µs/div to 1 s/div. Input coupling is AC or DC, and triggering is Auto, Normal, and Single. There are several trigger modes: rising/falling edge, pulse width, and level.

The DSO Quad uses an ARM Cortex-M3 (32-bit) processor and integrated FPGA with a high-speed ADC. There's an internal 2-Mbyte USB-connectable RAM for waveform storage and instrument setups. The 3-in. screen displays channel and setup information along the top and displays automatic measurements (V_{MIN}, V_{MAX}, V_{PP}, V_{DC}, V_{RMS}, and V_{BATT}) along the right side. The unit can also perform channel math functions such as A+B and A–B. The user can control all of these instrument configurations through toggle switches and a row of buttons along the unit's top edge.

The DSO Quad oscilloscope is just about the size of a standard business card and only about 13 mm thick.

In addition to being a digitizing oscilloscope, the DSO Quad is also a signal source. It has two built-in signal generators, an 8-MHz variable-duty-cycle square-wave generator, and a 20-kHz function generator (sine, triangle, and sawtooth). These signals come out through a separate connector.

The DSO Quad is available through www.seeedstudio.com/depot (under "Hacking & Measurement"). The DSO Quad's firmware is open source, and an active group of beta testers and other hobbyists develop additional functionality and make bug fixes. You can download periodic firmware updates from the user group page and load them through the unit's mini-USB connector (bit.ly/KKHykt). A YouTube video demonstrates the basic operation (bit.ly/IJk5o0).

Ken Wyatt, Wyatt Technical Services

OP-AMP TEST

Understand key ADC specs

ADCs are the engines that drive digitized measurements. These devices are found in test and measurement products as well as equipment such as industrial and medical instrumentation. So, even if you don't design measuring equipment but just use it, you should have an understanding of the specs that affect an ADC's performance.

Noise, ENOB (effective number of bits), and effective resolution are three important ADC parameters. These parameters become more significant as measurement products and systems move from SAR (successive-approximation register) ADCs, which typically produce 12 bits and 16 bits, to sigma-delta ADCs, which produce up to 24 bits.

As the number of bits increases, noise plays an increasingly important role, because the voltage range of each bit shrinks. A given noise level that has essentially no effect on a 12-bit ADC has a significant effect on a 24-bit ADC. On top of that, ADCs run at ever-smaller voltage ranges, and they may need PGAs (programmable-gain amplifiers), which amplify noise as well as signals. Noise, therefore, reduces ENOB and effective resolution, which are defined as:

$$\text{ENOB} = \log_2 \frac{\text{Full-scale voltage range}}{\text{ADC full-scale noise} \times \sqrt{12}}$$

and

$$\text{Effective resolution} = \log_2 \frac{V_{\text{IN}}}{V_{\text{RMS NOISE}}}$$

Sigma-delta ADCs oversample a signal, then apply filtering and data decimation to achieve their final outputs. That technique, shown in the **figure,** lets the converter reduce noise. A designer can optimize the ADC by making tradeoffs between

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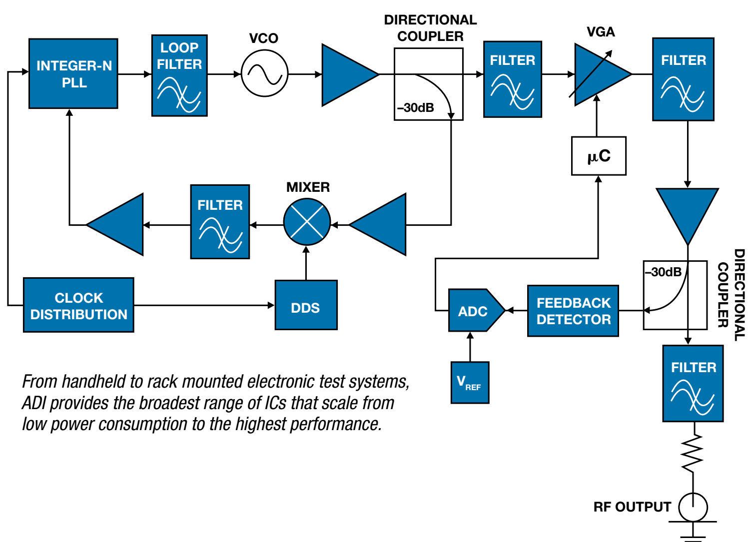
  Ultralow noise, integrated precision reference amp; speeds designs, reduces board space by 60%.
- **ADL5565: Differential RF/IF amplifier**
  Industry-best distortion levels; perfect for driving high performance 12- to 16-bit ADCs.

Frequency Translation Loop Signal Chain



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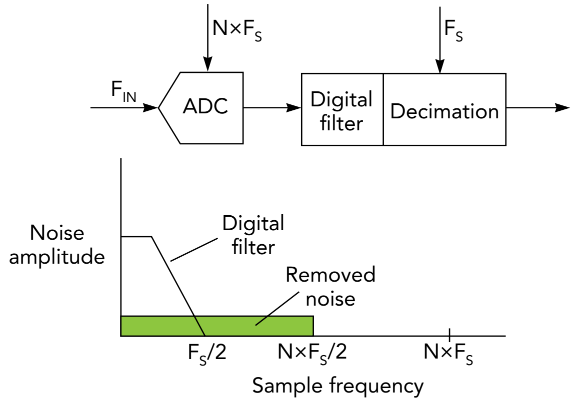
sampling speeds and noise performance when setting the oversample rate. To learn more, see "Understanding noise, ENOB, and effective resolution in analog-to-digital converters" by Steve Logan of Maxim Integrated products in the online version of this article: www.tmworld.com/2012_06.

Martin Rowe, Senior Technical Editor



A sigma-delta ADC oversamples a signal, then applies digital filtering and data decimation to produce the final digitized representation of the analog input.

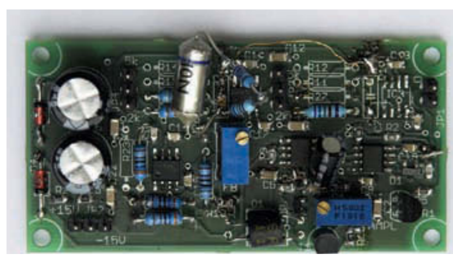
AUDIO TEST

Build a circuit to test ADCs

Today's 20-bit to 24-bit ADCs need low-distortion signals for testing how well the ADCs digitize analog signals. Distortion in the source signal will add to any distortion that the ADC produces. Thus, low-noise signals are critical.

When he couldn't find an oscillator with sufficiently low distortion, Vojtěch Janásek, an engineer at Janascard in the Czech Republic, built his own. The **figure** shows the oscillator, which produces distortion that's more than –140 dB below the oscillator's fundamental output signal. In addition, Janásek designed a notch filter that removes the oscillator's fundamental frequency. That lets him view the distortion produced by the ADC.

The oscillator uses an inverted Wien-bridge topology with amplitude stabilization through an LED-driven CdS (cadmium-sulfide) photocell isolator. Using SPICE simulations before building the circuit, Janásek showed how the oscillator's voltage noise-spectral density is highest at its resonant frequency, then falls at higher frequencies.



A low-noise oscillator is made from discrete components and op amps.

To verify the performance of his oscillator and filter, Janásek connected the final test signal to a data-acquisition system and frequency-analysis software. This particular module has a 14-bit ADC with a 400-ksamples/s sample rate. The module averages eight samples to reduce sampling speed to 50 ksamples/s and takes 128 ksamples to perform spectral analysis. Janásek's measurement showed that the circuit's THD (total harmonic distortion) is –145 dB.

The online version of this article (www.tmworld.com/2012_06) contains a link to Janásek's article "Low-distortion oscillator tests measurement circuits," which includes schematics for both the oscillator and filter circuits, plus plots of their performance.

Martin Rowe, Senior Technical Editor

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Handheld Spectrum Analyzers (HSA)

Key Specs	N9344C	N9343C	N9342C
Frequency	1 MHz–20 GHz	1 MHz–13.6 GHz	100 kHz–7 GHz
DANL	-155 dBm/Hz	-155 dBm/Hz	-164 dBm/Hz
Sweep time	< 0.9 s	< 0.7 s	< 0.4 s
Weight with battery	3.6 kg (7.9 lbs)	3.6 kg (7.9 lbs)	3.6 kg (7.9 lbs)

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Cell-aware ATPG test methods improve test quality

Using cell-aware automatic test-pattern generation and simulation, you can find defects that other methods might miss.

BY RON PRESS, MENTOR GRAPHICS

Traditional IC pattern-generation methods focus on detecting defects at gate terminals or at interconnects. Unfortunately, a significant population of defects may occur within an IC's gates, or cells. Many internal defects in cells can be detected with traditional test methods, but some require a unique set of stimulus to excite the defect. A cell-aware ATPG (automatic test-pattern generation) method characterizes the library cell's physical design to produce a set of UDFMs (user-defined fault models). Thus, the method uses the actual cell-internal physical characteristics to define and target faults.

In addition to explaining how cell-aware ATPG works, I'll also use published simulation results from two major IC companies to highlight the test method. Production silicon test results using cell-aware UDFM have shown notable improvement in DPM (defects per million) beyond what stuck-at and transition patterns detect. As a result, cell-aware UDFM is garnering attention from manufacturers in the semiconductor industry.

A brief history of IC test

"Defects" are the actual problems or production issues that cause an IC not to function properly. "Faults" are models that try to represent defects with simple properties that correlate to defects and are easy for ATPG tools to use.

When ICs were first developed, their functions were fairly simple, and tests simply checked the IC's functional operation. An engineer would design a "functional test" that checked whether the IC functioned as intended.

As IC technology advanced, it became impractical for an engineer to manually create a thorough functional test for the device. Increasing sequential logic such as flops and latches within ICs further complicated functional test. It could take many tens of thousands of clock cycles to propagate data at the IC's input through the sequential logic, so it became almost impossible to create a functional test that could execute in a reasonable time and provide a high level of detection for all possible defects.

The solution was to implement scan DFT (design-for-test) structures within the device. Scan logic essentially turns sequential logic into shift registers, which are control-and-observe points that a tester can load and observe. The remaining test problem is the combinational logic between the sequential logic. Thus, the entire design is turned into many sets of small combinational logic surrounded by virtual control-and-observe points. This situation lends itself to automation using scan ATPG tools. Scan testing is considered a "structural test," because the logic gate segments are tested without specific tests of the intended function of the IC.

ATPG circumvents the need for detailed knowledge of the IC design. The scan structure also produces very high defect detection. Standard scan testing is based on a stuck-at fault model that considers a potential stuck-at-0 and stuck-at-1 fault at every gate terminal. The stuck-at fault model verifies that gate terminals are not "stuck" at logic-0 or logic-1 states.

Somewhere between the times when 130-nm and 90-nm process technologies were developed, new timing-related defects occurred that demanded special at-speed tests. One type of at-speed scan test, called transition patterns, was used to target and detect the timing-related defects. Like stuck-at scan tests, transition tests use scan cells as control-and-observe points. After a transition test loads the scan cells, however, it puts the IC in functional mode and applies two or more at-speed clock pulses.

Stuck-at and transition scan tests, therefore, are the foundation of most production test methods; they can be automated within ATPG tools, and they can achieve high test coverage because of their structural nature. In recent years, newer scan tests have been introduced to target defects that escape stuck-at and transition tests. Examples include timing-aware ATPG, deterministic bridge, multiple detect, and hold-time methods (Ref. 1). Each of these methods provides some amount of improved defect detection.

All of these scan test methods use fault models that define fault sites at the IC gate boundary. Stuck-at-fault models, however, also detect the majority of production defects such as bridges, opens, and even many defects within the gates. With more recent fabrication technologies, the population of defects occurring within cells is significant, perhaps amounting to roughly 50% of all defects (Ref. 2). Thus, it is important to ensure that you properly define fault models that target these "cell-internal" defects.

Cell-aware ATPG

To target the cell-internal defects, test engineers can now use the physical design of gate cells to drive ATPG. This involves performing a library characterization to determine where defects can occur and how they would affect the operation of each cell. The result of the characterization is a UDFM that describes all the cell inputs and responses necessary to detect the characterized defects. A cell-aware UDFM file would be produced for a physical library for a particular technology. Then, any design using that technology library just needs the corresponding cell-aware UDFM file for cell-aware ATPG.

UDFM is a term used to describe an ATPG tool capability that lets you custom-define fault models. You might want to use a UDFM for ATPG if there is a particular type of pattern that you want to apply to a library cell, to an instance, or between instances. The definition of the UDFM is similar to stuck-at and transition patterns. You state the values at the cell or instance inputs and indicate what the expected response is for any number of desired cycles. Once the ATPG tool loads the UDFM file, it can target the custom-defined faults. UDFM provides the framework for many types of custom fault types.

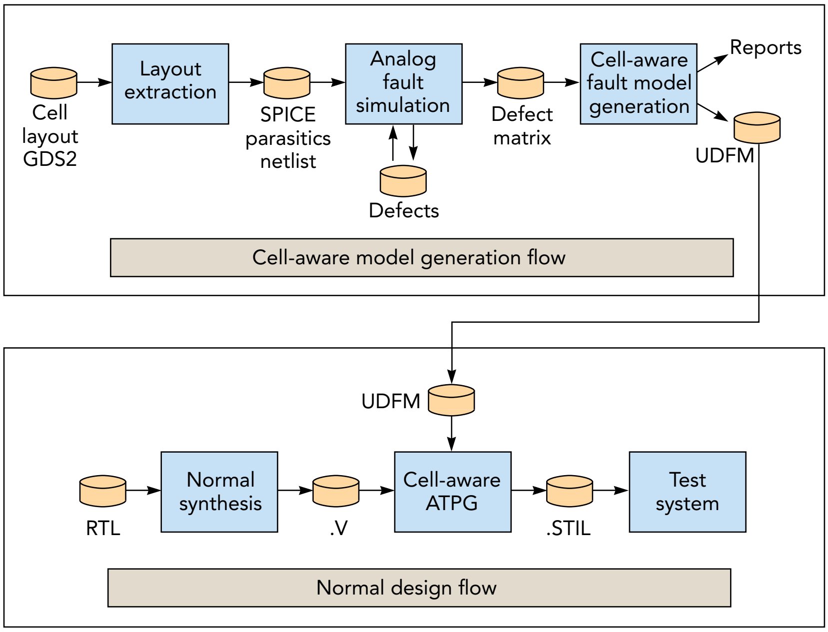


FIGURE 1. A cell-aware characterization generates a user-defined fault model for an ATPG flow.

Cell-aware characterization flow

The first step in creating cell-aware tests is to characterize the cells within a technology library. First, you must perform extraction on the physical cell layout library. Then, you can use the parasitic capacitances and resistances to locate potential sites for bridges and opens. (Capacitors represent potential bridges, and resistors represent potential opens.) Next, you define the type of defects you want to model. For example, a basic hard short can be modeled by a 1-Ω resistive bridge at the capacitor locations. Studies have shown value in modeling several resistive bridge values (Refs. 3 and 4).

With the definitions in place, you can perform an analog fault simulation with the desired defects, such as a 1-Ω bridge. The simulation is performed on all possible input combinations with one defect site at a time. The results are compared to the defect-free responses. If any of the responses differ from those for the defect-free case, then that sequence is said to detect the particular defect. Once you perform the analog simulation for all cell-input sequences, for all defects being modeled, and for all cells in the library, you will have a defect matrix. Finally, you can use the defect matrix to generate the actual cell-aware UDFM file used by ATPG. **Figure 1** shows the cell-aware characterization and ATPG flow.

Cell-aware ATPG makes a difference

Why is cell-aware ATPG necessary for finding defects that stuck-at and transition patterns presumably miss if production tests based on stuck-at and transition have been effective for many years? The need for cell-aware ATPG arises from the increased use of complex cells and the growing distribution of defects occurring within those cells.

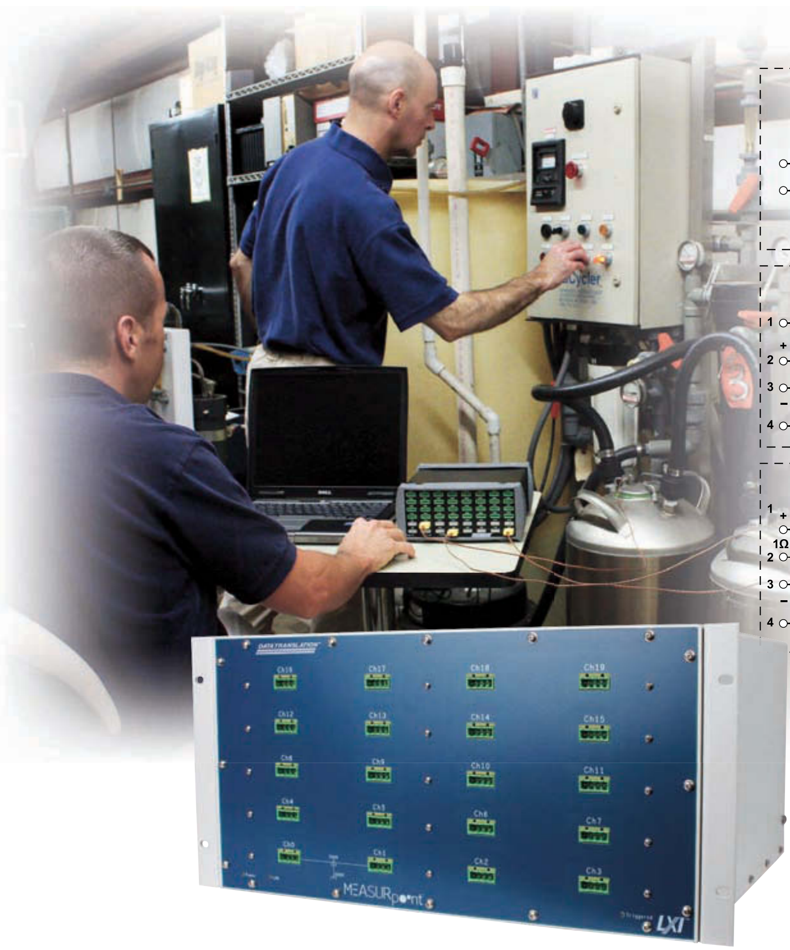
Many library cells won't see any advantage to performing cell-aware ATPG compared to normal stuck-at or transition ATPG. For example, a buffer, an AND gate, or an OR gate needs no special inputs to detect cell-internal defects. Consider a 3:1 mux gate. **Table 1** shows the logic table for the mux. These are the values that are needed to detect all stuck-at faults (stuck-at 1 and 0 at each cell boundary pin). *(continued)*

Table 1. Logic table for 3:1 mux.

S0	S1	D0	D1	D2	Z
0	0	0	–	–	0
0	0	1	–	–	1
1	0	–	0	–	0
1	0	–	1	–	1
–	1	–	–	0	0
–	1	–	–	1	1

Table 2. Cell-aware values necessary to detect a bridge at R4 (see Figure 2).

S0	S1	D0	D1	D2	Z
0	0	0	–	1	0
1	0	–	0	1	0
0	1	1	–	0	0
1	1	–	1	0	0



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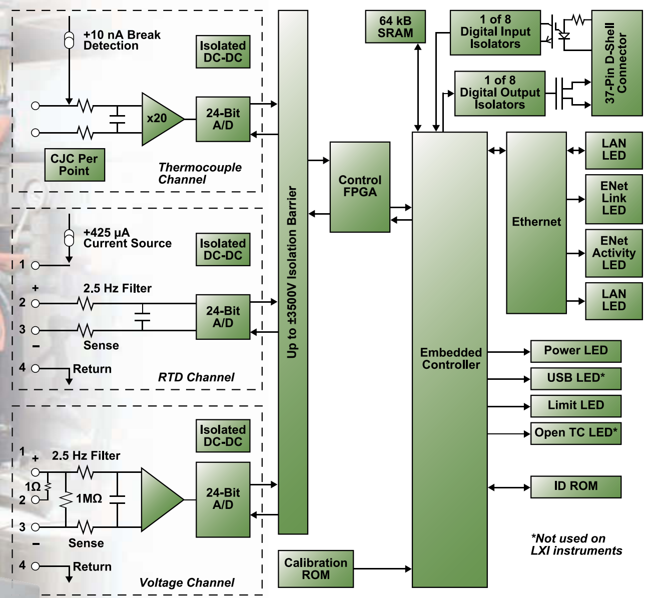
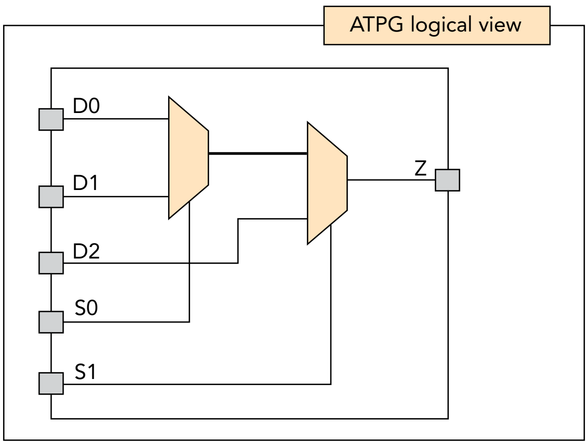


+10 nA Break Detection
Isolated DC-DC
x20
24-Bit A/D
CJC Per Point
Thermocouple Channel
+425 µA Current Source
Isolated DC-DC
2.5 Hz Filter
Sense
Return
24-Bit A/D
RTD Channel
Isolated DC-DC
2.5 Hz Filter
1Ω
1MΩ
Sense
Return
24-Bit A/D
Voltage Channel
Up to ±3500V Isolation Barrier
Control FPGA
Calibration ROM
64 kB SRAM
1 of 8 Digital Input Isolators
1 of 8 Digital Output Isolators
37-Pin D-Shell Connector
Embedded Controller
Ethernet
LAN LED
ENet Link LED
ENet Activity LED
LAN LED
Power LED
USB LED*
Limit LED
Open TC LED*
ID ROM
*Not used on LXI instruments

Figure 2 shows the logical view that the ATPG uses along with the physical layout of the cell. In this layout, a bridge at location R4 could cause a short from S1 to D2. If a value on D2 dominates over S1 in the presence of a bridge, then the logic-test patterns might not detect the bridge at R4.

Although the pattern set in Table 1 will achieve 100% stuck-at coverage for the mux, it doesn't ensure that R4 or several other cell-internal bridges will be detected. In this case, the patterns in **Table 2** would be needed to detect the R4 bridge. Other complex gates would have similar situations.



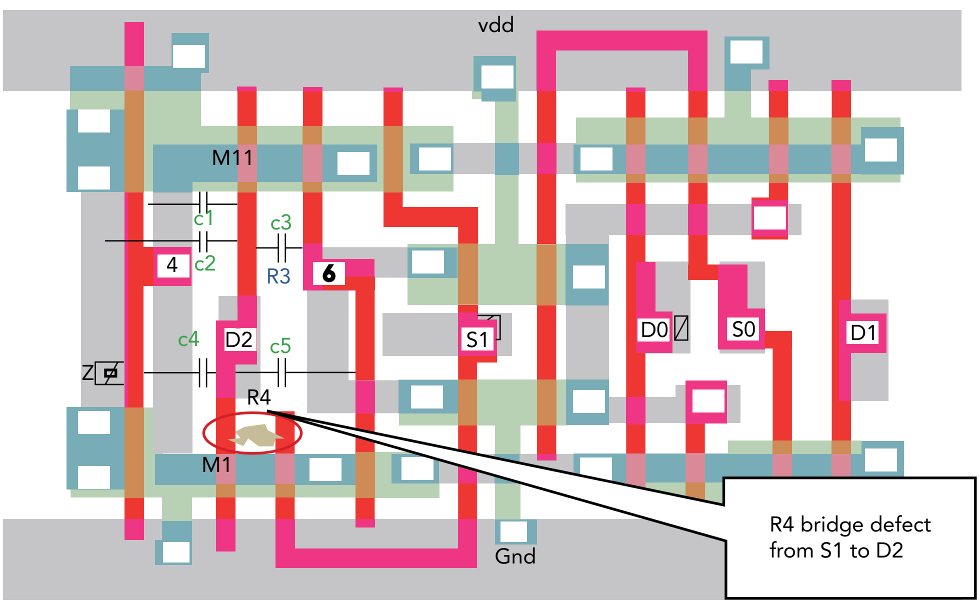


FIGURE 2. A 3:1 mux logical view (top) and layout (bottom) show a potential bridge defect.

Industrial results

Several IC companies have used cell-aware ATPG to improve defect detection. NXP Semiconductor used a cell-aware UDFM tool to perform cell library characterization and reported expected cell-internal detection improvement (Refs. 3 and 4). Published results can help you determine whether to model hard bridges such as a 1-Ω resistance or a variety of bridge values (Ref. 4). Cell-aware fault simulations on the 1-Ω bridge case showed an average of 1.2% cell-internal fault coverage improvement compared to stuck-at tests for 10 designs.

Bridges are the most popular type of modeled defect, but there are many types of defects that you can model using the cell-aware characterization. Another defect that some users are modeling is the internal opens defect (Ref. 4).

AMD published test results based on applying cell-aware patterns to 600,000 ICs using a 45-nm process (Ref. 5). The results showed that cell-aware patterns detected defects in 32 devices that passed stuck-at and transition patterns. That correlates to a 55 DPM improvement, which is significant for many production environments. More significant DPM improvements have been observed on a 32-nm process IC using slow-speed and at-speed cell-aware patterns.

Choosing the best tests

With cell-aware and other types of fault models and test types, you may have trouble deciding which and how much of each to use in production. Most IC test sets have stuck-at and transition patterns as a baseline. There are a few methods for choosing an effective pattern set. Effective and efficient production results require good data about the defect distribution and effectiveness of tests. Often, such data is not clear, because defect distributions vary with technology nodes, operational frequencies, slack margins, and design-for-manufacturability rules.

Here are two methods for determining an effective test set. Each requires some investment to apply the tests and determine their value:

- **Using field returns.** Field returns are devices that passed production tests and were shipped as functional, but that later failed. If you have a population of such devices, you can use them to find the value of additional tests. As a first step, retest the parts to ensure they didn't break after shipment.

You can apply a full set of tests for any type of potentially valuable test pattern. Then, use the percent detection and pattern set size to equate a relative value of the test type. For example, if you have 300 field returns from a production of 100,000 parts, then detecting 50 devices with cell-aware ATPG would imply you could improve DPM by 500 DPM, if cell-aware ATPG was part of production test. You can use a

similar approach if you have a thorough system-level test that finds defective parts that passed production test.

• **Adaptive tests for production.** Another approach is to add a set of additional patterns to the existing stuck-at and transition pattern sets. Often, there is not much spare room to apply new pattern sets in production. The additional patterns need not be complete sets. You can add 1000 patterns for each pattern type that you are interested in. After some volume of production test, you can observe the number of unique detects from each of your additional patterns. You can use these results to increase the pattern types that are detecting more defects and decrease the size of less-effective patterns.

Data from these tests gives you some insight into the defect distributions based on the DPM detection of tests and their calculated test coverage. From that, you can extrapolate the value of a full pattern set or the detection value of using a smaller pattern set.

The test pattern types that have shown the most promise beyond stuck-at and transition patterns are timing-aware and cell-aware. Gate-exhaustive tests apply every combination of inputs to each cell. They have good detection but are unreasonably large pattern sets. Cell-aware is a subset of gate-exhaustive patterns that only include stimulus combinations that can cause the modeled defects to be detected.

The new cell-aware ATPG flow allows test engineers to target subtle shorts and open defects internal to standard cells that are not adequately detected with the standard stuck-at or transition fault models. Cell-aware testing has been proved to increase the quality of manufacturing test by providing higher defect coverage and lower DPM. T&MW

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On-chip frequency measurements reduce test time

On-chip frequency measurements allow for concurrent, parallel, and faster frequency measurements.

BY SURBHI BANSAL AND SAMEER SARAN, FREESCALE SEMICONDUCTOR

Shrinking geometries and efficient design techniques are helping to reduce die sizes, which lowers the cost of semiconductor devices. Despite these improvements, increased competition and smaller gross margins are forcing semiconductor companies to reduce the overall cost of IC production even more. One of the major contributors to total device cost is the cost of testing.

For the digital portion of ICs, DFT (design for test) techniques have significantly reduced test complexity and test times. Unfortunately, testing the analog portion of an IC is much more complex. As a result, most engineers still perform analog measurements using conventional methods, such as bringing the analog output to a package-level pin and performing the measurement using external instruments. This approach has its disadvantages, especially in terms of time and cost.

Fortunately, there is a way to reduce the test time spent on clock frequency measurements. By performing on-chip frequency measurements, device manufacturers can reduce their dependency on external instruments and can perform concurrent, parallel, and faster frequency measurements without adding any significant silicon area. In fact, one study has shown a reduction in test time of more than 50%. For devices with many clock sources, this can lead to significant test cost savings.

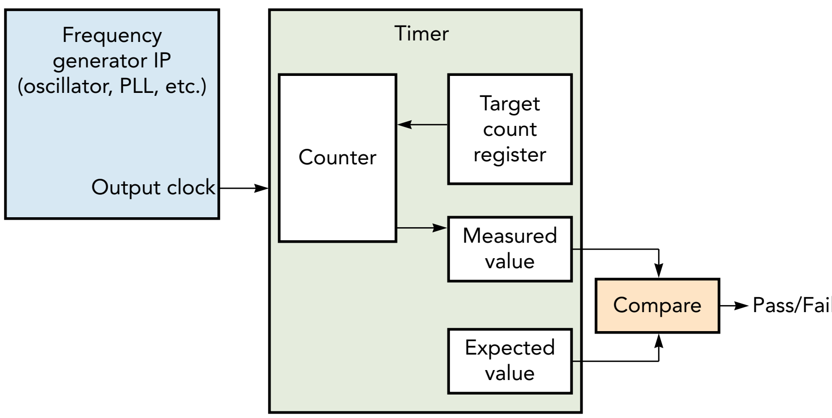

FIGURE 1. Frequency measurements can be performed using on-chip timers

Test challenges for ICs

As semiconductor geometries have shrunk, manufacturers have reduced the test time for the digital portion of their devices through the use of DFT techniques, which have led to increased scan compression and high scan-test coverage. Analog test time, however, remains high, because manufacturers typically still use conventional methods for analog tests.

For example, most MCUs (microcontrollers) now have internal on-chip oscillators and PLLs (phase-locked loops). In addition to measuring static parameters, engineers must test the chip's frequency output during production.

Engineers have traditionally measured frequency by bringing the output clock of the device through some clock dividers on an SOC (system-on-chip) pin output. Using the external frequency counters on ATE (automated test equipment), designers would measure the frequency, and the chip would pass or fail based on design specifications. This method has several limitations.

Table 1. Test time comparisons for a Freescale MCU.

Measurement method	Frequency to be measured	Target count (time)	Test time breakdown			Total test time
			Pre-test	Test	Post-test	
External	8 MHz	1.25 ms	3.3 ms	4.5 ms	65 ns	7.8 ms
External	32 MHz*					
On-chip	8 MHz	1.25 ms	0.2 ms	3.3 ms	65 ns	3.5 ms
On-chip	32 MHz	0.3125 ms	0.2 ms	2.36 ms	65 ns	2.56 ms

*May not be measurable if I/O pads don't support such high frequencies.

First, there is a frequency limitation of design. Since design I/O pads are usually low frequency, engineers must divide the output clock to be measured before exposing it to (or bringing it out to) the pin pad. Next, in order to achieve an accurate measurement, the test requires a significant number of clock cycles to be counted. Therefore, measuring a slow clock on ATE would mean longer test times. External test equipment also has a settling time, which influences the time to answer. In addition, some ATE platforms need a dedicated pin to be configured in frequency counter mode, rendering that pin useless for any other purpose in the test. Finally, the actual measurement resolution depends on the tester period.

You can overcome these limitations and reduce test time by eliminating the dependency on external equipment and by implementing faster frequency-measurement methods. To do that, you first must understand how an external tester performs a frequency measurement and then try to mimic this behavior on-chip.

The specific implementations of frequency measurements vary from tester to tester, but the typical measurement works by counting the number of rising edges of clock over a period of time and averaging it to find out the actual output frequency. The simple equation is:

$$frequency = count/period$$

where:
count = the number of rising edges counted in the specified period, and
period = time span of the test.

To eliminate dependency on pin-based measurements using external test equipment, you must find a way to count the number of rising edges of output clock inside the chip, and then store, post-process, and decide on a pass/fail result.

DFT technique

Most MCUs are equipped with real-time counters, timers, or high-bit positive-edge detectors. In our proposed frequency-measurement method, we strap the output clock to the on-chip timer input and then set the required time duration in timer registers (target count register). The on-chip timer counts the target clock rising edges during the specified period.

After the timer counter reaches the time duration set in the register, it will output the digital count of the clock, which can be compared internally to declare if the chip passes or fails (**Figure 1**). Also, we can connect the digital result of the timer to a device pin in order to report the clock frequency value.

In this method, the clock under test does not need to be divided, because it is not brought out directly to the primary I/O pin. (But the timer frequency must be at least two times faster than the clock being measured.) The number of cycle counts for the clock will be the same as in the conventional method. For faster clocks, the cycle counts can remain the same as for slower clocks, but since the clock is faster, it takes less time to reach the same count. This leads to significant reduction in test time and reduces the device test cost.

The method requires no special tester hardware, as the device is being tested internally. Therefore, you don't need to account for the settling time of the tester hardware when planning your tests.

The on-chip method has several advantages. First, you can perform the on-chip test at any test insertion without adding extra pins for output frequency. If you perform the test at the wafer level, you won't need any high-frequency capable probes. Also, you don't have to be concerned about the capability of the tester, and the results are independent of the frequency characteristics of the I/O pads. Finally, even though it is a DFT technique, it does not add any significant silicon area, and no special hardware is required.

Table 1 shows a comparison between external and on-chip methods of frequency measurements. We collected the data on one of the MCUs from Freescale Semiconductor's Industrial and Mass Market portfolio using an industry-standard tester platform. A comparison of an 8-MHz clock measurement using the two methods under the same test and device conditions shows a test time reduction of more than 50%.

External measurement techniques work well enough for frequencies that are within the I/O spec. In the case where the frequency is too high, it will need to be divided inside the chip and then measured. The proposed on-chip method provides an excellent and faster alternative to external frequency measurements. T&MW

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Sameer Saran *is lead test engineer at Freescale Semiconductor India. His expertise is in the areas of mixed-signal testing, innovative test strategies, and test cost reduction.*

Introduction to IEEE 802.11ac manufacturing test requirements

BY ROBIN IRWIN, AEROFLEX

As WLAN standards evolve, manufacturers need to ensure their test equipment can support 802.11ac test requirements as well as legacy and complementary technologies.

IEEE 802.11ac is a draft WLAN standard aimed at delivering VHT (very high throughput) local wireless connectivity. The proposed standard supports data rates that are up to 10 times faster than those of WLAN 802.11n HT (high throughput), and it also specifies a signal bandwidth of up to 160 MHz (four times that of 802.11n). In addition, 802.11ac will support MIMO (multiple-input, multiple-output) communications with up to eight data streams.

Chipset vendors are already releasing reference designs for 802.11ac that have an 80-MHz bandwidth, and many observers expect that the 160-MHz capabilities will be adopted over time in the same way that 802.11n evolved into more complex and effective MIMO implementations.

Engineers who are responsible for developing and performing manufacturing tests should understand how WLAN standards evolve in order to plan for future testing. For example, 802.11ac test equipment will need wide-bandwidth analysis and generation capabilities in order to handle the mandatory 80-MHz channel bandwidth. For those familiar with testing 802.11n devices, the test requirements for 802.11ac have many similarities.

The test setup

When 802.11n was introduced, manufacturers needed a test setup that could evaluate multiple antennas for MIMO. This presented manufacturing test engineers with a new challenge: finding a way to test MIMO radios while maintaining the same cost of test and with minimal impact to test time and test throughput.

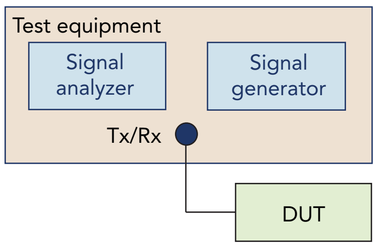

FIGURE 1. This basic test setup can be used to perform IEEE 802.11ac WLAN testing.

Fortunately, 802.11ac has similar MIMO requirements, so existing 802.11n test setups are applicable. In a typical setup (**Figure 1**), the signal analyzer provides the means of Tx (transmitter) testing, while the signal generator delivers the output required for Rx (receiver) testing. For the sake of simplicity, the test equipment in this example is configured to present one RF port (Tx/Rx) to the device that can potentially test one of the following scenarios:

- a single 802.11ac SISO (single input, single output) device (1×1) with one RF chain/radio, or
- a single 802.11ac RF chain/radio on a MIMO device ($n \times m$), testing each chain as a separate radio on the device (n transmitters can be tested in turn, for example, by sequentially switching to each chain in turn).

Testing more than one device in parallel would require additional hardware—something that is easy to add if the test setup is based on modular equipment.

The test plan

Similar to an 802.11n test plan, an 802.11ac test plan is likely to include a

Table 1. IEEE 802.11ac test requirements.

	Test name	Reference
Transmitter testing	Transmit spectrum mask	22.3.18.1
	Spectral flatness	22.3.18.2
	Transmit center frequency tolerance	22.3.18.3
	Symbol clock frequency tolerance	22.3.18.4
	Transmit center frequency leakage	22.3.18.5.2
	Transmitter constellation error	22.3.18.5.3
Receiver testing	Receiver minimum input sensitivity	22.3.19.1
	Adjacent-channel rejection	22.3.19.2
	Nonadjacent-channel rejection	22.3.19.3
	Receiver maximum input level	22.3.1.4

range of tests that cover the expected use of the device. In the same way that 802.11n test plans contained test items that allowed a device to operate in both legacy and HT modes, an 802.11ac test plan will do the same to address backward compatibility (an important feature of the specification).

Even though the test must test backward compatibility, engineers will likely focus on testing 802.11ac signals. For example, engineers are likely to define spectral-mask requirements for at least an 80-MHz transmission and verify modulation accuracy at MCS (modulation and coding scheme) 9 for 256 QAM, with receiver testing also using an 802.11ac MCS 9 signal.

The specific test items contained within a test plan are very similar to 802.11n. **Table 1** includes a list of test items from the standard (Ref. 1).

Note that adjacent-channel-rejection and nonadjacent-channel-rejection tests require an interfering signal from an additional signal generator. These tests are verified prior to manufacturing and are not considered a production test requirement, so they are not covered in this analysis.

Transmitter tests

The 802.11ac draft standard specifies six Tx tests:

•**Transmit spectrum mask.** The spectral mask test verifies that the output spectrum from the device does not interfere with other devices, and that the spectrum meets the mask requirements set in the specification. This test is typically performed at maximum power output from the device. **Figure 2** and **Table 2** summarize the requirements for each signal bandwidth.

The engineer should check that the spectrum meets the dBr (decibels relative to reference level) mask requirements where they are relative to the maximum spectral density of the signal. Or, depending upon the power level of the input signal, the engineer should check the dBm/MHz requirement (which dictates the highest mask value allowed).

Taking the maximum of either requirement addresses the 802.11ac specification. In each case, the engineer needs to make the measurements using

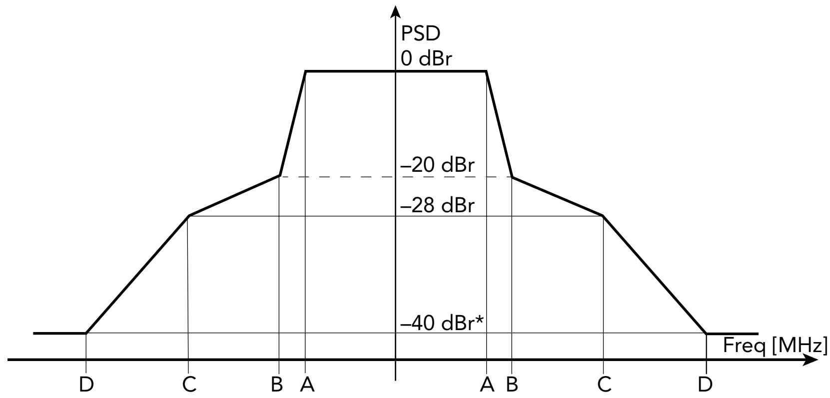

FIGURE 2. Spectral-mask requirements are dependent on signal bandwidth.

Table 2. Signal bandwidths for spectral-mask requirements.

Signal bandwidth under test	Reference to Figure 2				Test limit
	A	B	C	D	Maximum of:
20 MHz	9	11	20	30	–40 dBr and –53 dBm/MHz
40 MHz	19	21	40	60	–40 dBr and –56 dBm/MHz
80 MHz	39	41	80	120	–40 dBr and –59 dBm/MHz
160 MHz	79	81	160	240	–40 dBr and –59 dBm/MHz

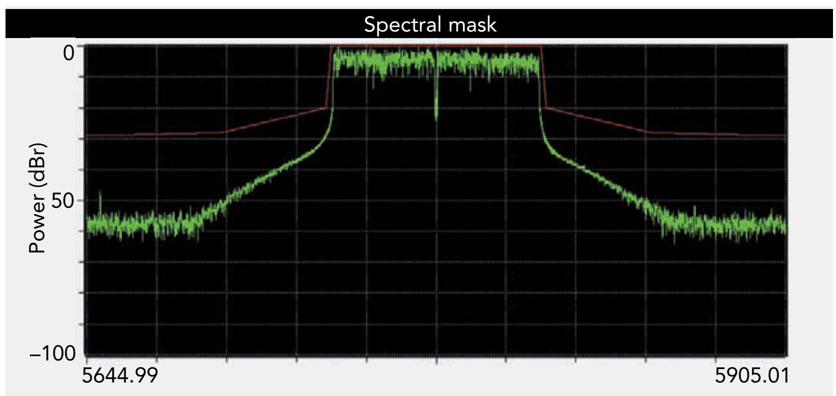

FIGURE 3. An MCS 8 80-MHz signal demonstrates spectral-mask performance.

Table 3. 80 + 80-MHz noncontiguous spectral mask values.

Mask region (per Figure 2)	Frequency overlap	Resultant mask value
0 dBr to –20 dBr (A–>B)	Neither (not possible)	Higher of the two masks
–20 dBr to –40 dBr (B–>D)	Both masks	Sum of both masks (linear)
Other	Any frequency region that has not been defined in the above	Linear interpolation (dB) between two nearest frequency points with defined mask values

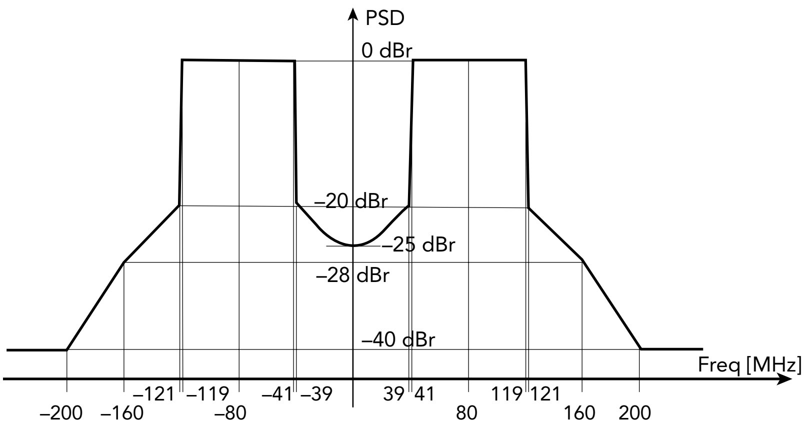

FIGURE 4. **The IEEE 802.11ac draft specification provides a noncontiguous spectral mask example with two center frequencies 160 MHz apart.**

a 100-kHz resolution bandwidth and a 30-kHz video bandwidth. **Figure 3** shows an example measurement for an MCS 8 80-MHz signal.

Finally, the specification describes the procedure for the 80 + 80-MHz noncontiguous case. The mask is constructed from two 80-MHz masks that are then combined or overlapped. The mask limits are calculated as shown in **Table 3**. The specification provides an example of this with two center frequencies separated by 160 MHz (**Figure 4**).

For a spectral-mask measurement, the engineer should be able to use the test setup, which will include a signal generator, signal analyzer, and software options, to define the mask required, and then the equipment should return (as a minimum) a pass or fail versus the mask.

• **Spectral flatness.** Spectral flatness is a measure of the deviation of each subcarrier from the average power. You can measure spectral flatness using BPSK (binary phase-shift keying) modulated packets. As the measurement is dependent on the signal bandwidth in question, the specification limits are defined per subcarrier.

Table 4. Spectral flatness subcarrier indexes by bandwidth of transmission.

Bandwidth	A	B	C
20 MHz	1	17	28
40 MHz	2	43	58
80 MHz	2	85	122
160 MHz	N/A (limit is +4/–6)	6	250

Figure 5 illustrates $E_{i,avg}$ as the average constellation energy of a BPSK modulated subcarrier, i, in a VHT data symbol. The mask limits in each case (shown in red) are ±4 or –6 depending upon whether the reference is to the central region (–B to B) or the outer region (–B to –C and B to C) of subcarriers.

Table 4 provides the subcarrier indexes depending upon the bandwidth of the transmission. Note that subcarrier position B represents the start of the outer region (inclusive). The 160-MHz bandwidth does not use the −4-dB limit. An example of a measurement for an 80-MHz signal is shown in **Figure 6**.

• **Transmit center frequency tolerance.** This test looks at the frequency error (with respect to the desired carrier frequency) from the transmitter, normally produced as a demodulation of the modulated signal. The criteria for a pass is < ±20 ppm (0.002%). As an example, this would be ±275 kHz at 5500 MHz.

• **Symbol clock frequency tolerance.** The symbol clock frequency tolerance is a measure of the symbol clock frequency offset from the desired symbol clock frequency. The pass criteria is < ±20 ppm. This test checks for any time-varying frequency changes in the local oscillator. If the fre-

Table 6. Permitted transmitter constellation error.

MCS	Modulation	Coding rate	Relative constellation error (dB)
0	BPSK	1/2	–5
1	QPSK	1/2	–10
2	QPSK	3/4	–13
3	16 QAM	1/2	–16
4	16 QAM	3/4	–19
5	64 QAM	2/3	–22
6	64 QAM	3/4	–25
7	64 QAM	5/6	–27
8	256 QAM	3/4	–30
9	256 QAM	5/6	–32

Table 5. Transmit center frequency leakage test conditions and limits.

Test condition	Test limits
RF LO center of transmitted PPDU bandwidth	Power measured at center <P_T –10log(N)
RF LO not center of transmitted PPDU bandwidth	Power measured < maximum of (P_T – 32 dB, –20 dBm)
Noncontiguous, nonadjacent 80-MHz channel, RF LO outside both channels	Spectral mask requirements 22.3.19.1

Note: PT = total transmit power; N is data plus pilots tone; resolution bandwidth is 312.5 kHz.

quency error is measured, there is no need to return this measurement.

• **Transmit center frequency leakage.** The transmit center frequency leakage test is designed to check for any unwanted energy at the center frequency of a modulated signal. This leakage can sometimes cause problems for receivers.

Leakage is defined according to three conditions depending upon the position of the LO (carrier). For example, an LO would not be in the center of a transmission bandwidth if a 20-MHz or 40-MHz transmission was used in an 80-MHz channel (**Table 5**).

• **Transmitter constellation error.** Together, transmitter constellation error and transmit center frequency leakage (which applies to all bandwidths) form the requirements for testing the modulation accuracy of the transmitter. The specification states that the number of spatial streams under test shall be equal to the number of antennas and also to the number of input ports on the test equipment. **Table 6** shows the RCE (relative constellation error) in decibels for the different MCSs. The measured result should not exceed the data-rate dependent value.

The payload data must be random and be at least 16 data OFDM (orthogonal frequency-division multiplexing) symbols long. The test must be performed over at least 20 frames. An example of modulation accuracy results for an MCS 8 signal returning an RCE is shown in **Figure 7**, and the constellation is shown in **Figure 8**

Receiver testing

During Rx testing, each measurement result is reported from the device itself. Test engineers must set up the test equipment with the correct signal for stimulation of the Rx tests.

Many test vendors offer signal-generation packages that engineers can use to design specific WLAN signals. In general, most chipsets and commercial devices are set up during the manufacturing process so they need very little in the way of specific receiver parameters. The most commonly needed setup steps involve adjusting the size of the data and perhaps using a specific MAC address. **Table 7** contains an example

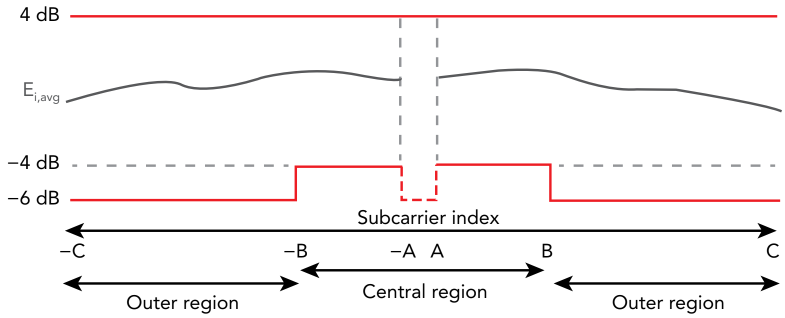

FIGURE 5. The spectral-flatness test requirements show $E_{i,avg}$ as the average constellation energy of a BPSK modulated subcarrier, i, in a VHT data symbol.

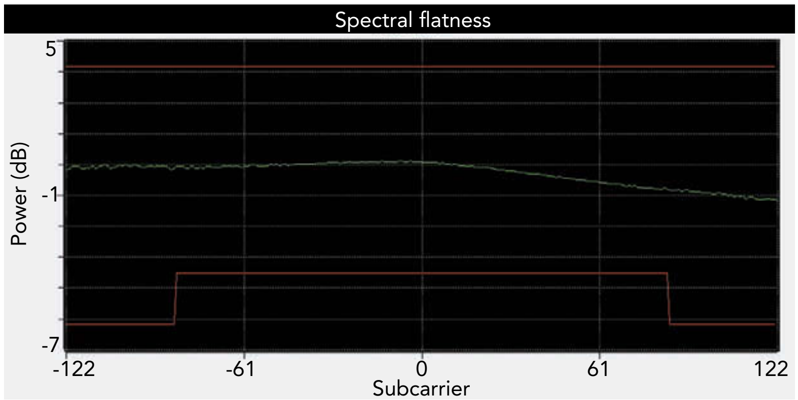

FIGURE 6. An 80-MHz signal returns this spectral-flatness measurement.

Modulation Accuracy							
	Antenna 1				Antenna 1		
	Live	Average	Std. Dev.		Live	Average	Std. Dev.
System Type	OFDM	-	-	Modulation Type	256QAM	-	-
Data Rate	351 Mbps	-	-	HT Format	N/A	N/A	N/A
MCS	8	-	-	Short GI Detected	False	-	-
Cross Power	N/A	N/A	N/A	EVM RMS	0.568 %	0.578 %	0.024 %
EVM Peak	N/A	N/A	N/A	EVM Data Carriers	0.569 %	0.578 %	0.025 %
EVM Pilot Carriers	0.539 %	0.566 %	0.053 %	Frequency Error	71 Hz	16 Hz	126 Hz
Symbol Clock Error	0.228 ppm	0.112 ppm	0.080 ppm	Carrier Leak	-50.416 dB	-50.623 dB	0.399 dB
IQ Gain Imbalance	0.031 dB	0.031 dB	0.003 dB	IQ Skew	0.017 °	0.031 °	0.016 °
Number of PSDU Bits	22442	22442	0	Number of PSDU Symbols	16	16	0
RCE RMS	-44.906 dB	-44.776 dB	0.352 dB	RCE Data Carriers	-44.891 dB	-44.772 dB	0.357 dB
RCE Pilot Carriers	-45.364 dB	-44.987 dB	0.804 dB				

FIGURE 7. These are the modulation accuracy results for an MCS 8 signal.

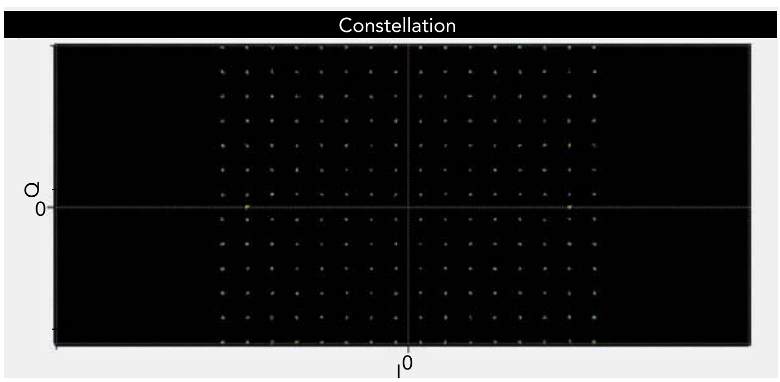

FIGURE 8. This constellation diagram shows the results from Figure 7 for the MCS 8 256 QAM signal.

Table 7. Example requirement for an MCS 7 64 QAM 5/6 coding rate.

Standard: IEEE 802.11ac
Channel bandwidth: 80 MHz
MCS index: 7
Spatial streams: 1
Tx antennas: 1
Data: 400 symbols
Idle time: 1 µs

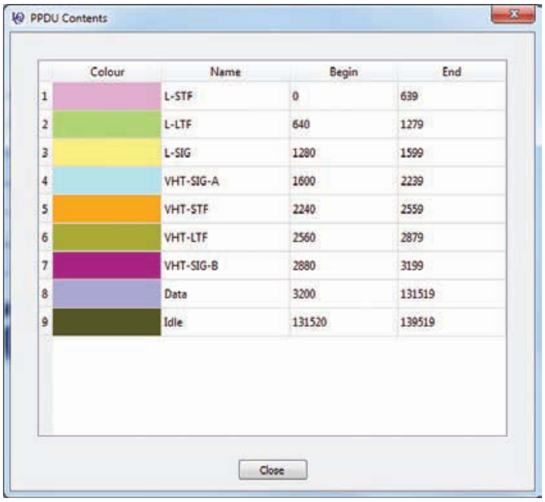

FIGURE 9. Engineers can configure the data field with a signal-design package, which will verify the PPDU.

requirement for an MCS 7 64 QAM 5/6 coding rate.

Starting with the data field, you need to understand what 400 symbols equate to for an MCS 7 signal. The number of octets to be defined depends on MCS. According to Table 22-41 in the draft standard (Ref. 1), for one stream with an 800-ns guard interval, there are 1170 bits per OFDM symbol, which is 146.25 octets. For 400 symbols, this equates to 58500 octets. The data source is likely to be PRBS9 as per the 802.11ac specification. The engineer can enter these parameters into a signal-design package, which will verify the PPDU (physical layer convergence procedure protocol data unit).

This analysis (**Figure 9**) shows that the data field begins at chip 3200 and ends at chip 131,519, which equals 128,320 chips. For an 802.11ac VHT signal with an 80-MHz channel bandwidth and a sampling rate of 80 Msamples/s, the duration of one marker chip is 0.0125 µs. With 4 µs per symbol for OFDM, there are 320 chips per symbol. For 400 symbols, this equals 128,000 chips, so the value determined for the data field looks correct. In fact, it is one symbol (320 chips) longer once designed and packaged.

A common requirement is to set up WLAN signals with a broadcast MAC header. IEEE 802.11 2007 (Ref. 2) contains a table that shows how to set up a beacon (**Figure 10**). This example shows that the bits b4 to b7 need to be configured for a beacon in order to define the subtype field in the frame control. The easiest way to do this is to use least-significant bit notation and enter "0000000100000000" into the frame control field of a signal-design package (**Figure 11**). If the engineer then selects and configures any other parameter required, the signal can be generated and packaged for playback for the specified receiver tests:

- **Receiver minimum input sensitivity.** Minimum input sensitivity testing is a key verification test of the ability of the receiver to successfully demodulate an 802.11ac signal. The PER (packet error rate) should be less than 10% for a PSDU (physical layer service data unit) length of 4096 octets.

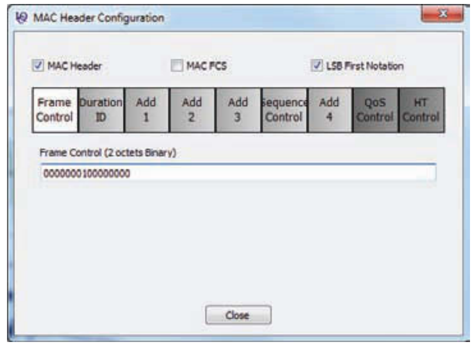

FIGURE 11. Designers can enter 0000000100000000 in a signal-design package for a MAC header configuration for broadcast mode.

a) Valid type and subtype combinations

Type value b3 b2	Type description	Subtype value b7 b6 b5 b4	Subtype description
00	Management	0000	Association request
00	Management	0001	Association response
00	Management	0010	Reassociation request
00	Management	0011	Reassociation response
00	Management	0100	Probe request
00	Management	0101	Probe response
00	Management	0110 0111	Reserved
00	Management	1000	Beacon

b) Frame-control fields

B0 B1	B2 B3	B4 B7	B8	B9	B10	B11	B12	B13	B14	B15
Protocol version	Type	Subtype	To DS	From DS	More frag	Retry	Pwr Mgt	More data	Protected Frame	Order
Bits: 2	2	4	1	1	1	1	1	1	1	1

FIGURE 10. a) The IEEE 802.11ac draft standard defines valid type and subtype combinations. Bits b4 to b7 need to be configured for a beacon in order to define the subtype field in the frame control (b).

The specification suggests 4096 octets. Taking MCS 7 as an example, there are 1170 bits per OFDM symbol for an 800-ns guard interval, which is 146.25 octets, so 4096 octets is just over 28 symbols. For MCS 9 this is just over 21 symbols.

• **Receiver maximum input level.** In contrast to the minimum sensitivity test, this test makes sure that the device can receive when the power level incident to the antenna is comparatively high. The specification asks for this test to be carried out with a PSDU of 4096 octets using any MCS signal but at the higher power of –30 dBm. The test limit is again 10% of the PER.

Being test-ready for 802.11ac

Test equipment for 802.11ac must be able to test 80 MHz at a minimum, and should be able to evolve to test 80 + 80-MHz and 160-MHz scenarios. Some test equipment deployed in cellular and noncellular manufacturing lines for signal generation and signal analysis already supports an 80-MHz bandwidth. For this equipment, the upgrade path for 802.11ac testing is easier, and the necessary capabilities can be added through software upgrades. The 160-MHz bandwidth presents a different challenge, however, and hardware upgrades are necessary.

Just like 802.11a/b/g/n, 802.11ac is unlikely to be the only technology a manufacturer is concerned with testing. Indeed, end products such as mobile phones may offer WLAN as a complementary technology. In the early days of WLAN, manufacturers often used dedicated WLAN test equipment. Over time, however, as chipsets offered WLAN alongside technologies such as Bluetooth, GPS, FM, and WiMAX, manufacturers needed test equipment that could handle a breadth of cellular formats. Manufacturers can no longer support a range of test platforms for a mix of technologies. A modular hardware and software platform can also bring further advantages. Using capable test equipment, engineers need to know about the new 802.11ac test requirements in order to understand what potential test plans can be deployed, how to address individual test cases, and how to fulfill these tests using available test equipment. T&MW

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Robin Irwin *is a senior applications engineer team lead supporting the PXI 3000 series of modular instruments for Aeroflex based in the UK. He provides global application expertise in manufacturing test for wireless multicommunications products. Irwin joined Aeroflex with over seven years of test and measurement experience and with a first class master's degree in electrical and electronic engineering from Queens University of Belfast.*

SPECIAL FOCUS: Power Sources and Analyzers

Agilent boosts SMU's voltage and current

Today's high-power devices need characterization at full voltage and full current. Furthermore, these devices have ever-shrinking on resistances. To meet these power needs, Agilent Technologies has boosted the output of its B1505A power device analyzer/curve tracer. The B1505A mainframe (bottom unit in photo) has new modules that produce voltage up to 10 kV and current to 1500 A. New internal modules produce 100 V/100 mA (B1511A), 3000 V (B1513A), and pulsed 1 A/30 V (B1514A).

The B1505A also has a milliohm-resistance-measurement capability to accommodate small on-resistance measurements. When characterizing high-power devices such as

IGBTs, the B1505A uses all four-wire measurements to minimize losses in probe wires. The pulsing capability avoids self-heating, which can alter a device's characteristics. For high-voltage measurements, the B1505A can produce pulses as small as 10 μs wide. Ultra-high-current tests can have pulses down to 50 μs. Its ability to measure temperature lets the B1505A monitor the temperature of a device under test. With this upgrade, the B1505A now synchronizes temperature, voltage, and current measurements.

New high-power devices such as those made from GaN also have problems with current collapse. In those tests, you apply a high voltage and measure the current in the device. To help with those measurements, you can use the N1267A high-voltage/high-current fast-switch option, which switches the system from voltage mode to current-measurement mode in time to capture collapsed current in the device.

Price range: $45,000 to $200,000. *Agilent Technologies, www.agilent.com/find/b1505a.*

(continued)

Multitest Kelvin contactor suits high-power test

Aimed at high-power IC test applications up to 500 A, the ecoAmp Kelvin contactor from Multitest is designed to meet the requirements of high-voltage and high-current testing. The contactor provides max-

imum loop inductance of 4.5 nH for lead pitches down to 0.5 mm, and it can be used from −60°C to +175°C. The ecoAmp accommodates QFP, SO, TO, and DPAK devices and power modules used in automotive and motor-control applications.

With a cantilever spring and hard gold coating, ecoAmp provides typical contact resistance of 30 mΩ. Other specifications include a maximum peak current of 160 A at 1% duty cycle and maximum continuous current of 8 A. In addition, ecoAmp is optimized to withstand high thermal stress during testing and has a lifespan of 1 million insertions.

Base price: approximately $5206. *Multitest, www.multitest.com.*

Sorensen SG Series DC power supply family grows

AMETEK Programmable Power has added a 50-V model to its Sorensen SG series of DC power supplies. Output voltages for the series now range from 0–10 VDC to 0–800 VDC, with current up to 2400 A and power up to 150 kW. The new 0–50-V model provides an output of up to 100 A at 5 kW in a single unit.

The SGA version of the power supply can be controlled through front-panel controls or a remote serial interface. Features include 10-

turn potentiometers, a 3.5-digit LED readout, front-panel overvoltage protection preview/adjustment and reset, and remote interface options.

The SGI version provides onboard controls, a constant power mode, and save-and-recall of instrument settings. With its ability to loop sequences, the SGI is able to handle repetitive testing.

AMETEK Programmable Power, www.programmablepower.com.

USB scopes offer extra features

The PicoScope 6400 family of USB oscilloscopes features three models with bandwidths of 250 MHz (Model 6402), 350 MHz (Model 6403), and 500 MHz (Model 6404). Each is available in an "A" version, which includes a function generator, and a "B" version, which includes an arbitrary-waveform generator. The A models produce sine, square, triangle, and DC signals; the B models produce signals at 250 Msamples/s with 16 ksamples of signal memory.

All models feature an improved USB streaming mode. When sampling rates are 10 Msamples/s and slower, the oscilloscopes can capture 100% of the data 100% of the time.

The 6400 series scopes sample at 5 Gsamples/s on one channel, 2.5 Gsamples/s on two channels, and 1.25 Gsamples/s on three or four channels. Acquisition memory is shared among all active channels and ranges from 128 Msamples (6402A) to 1 Gsample (6404B). All models also support decoding of CAN, LIN, FlexRAY, SPI, I2C, UART, and RS-232 protocols.

Base price: $3291. *Pico Technology, www.picotech.com.*

Microwave switching systems take on many relays

The GT-8900 series of microwave switching systems from Giga-tonics consists of two models, the GT-8901 and GT-8902. The GT-8902 is a 2U-high, full-rack version, while the GT-8901 is a half-rack-width model. Both have GPIB and LAN ports that let you automate testing and are available in 18-GHz, 26.4-GHz, and 40-GHz versions.

You can configure a GT-8900 system with SPDT, SP4T, SP6T, and DPDT microwave switch modules. All modules are available with or without terminations. Internal firmware keeps track of each time a relay opens and closes. In addition, the GT-8902 provides LEDs on the front panel that indicate the closure status of each relay, so you can confirm that the automation software is properly closing the desired relay.

The Giga-tronics software lets you manually open or close any relay by clicking on the screen. For automated tests, you can use LabView drivers, which come with source code that lets you modify the driver as needed.

Giga-tronics, www.gigatronics.com.

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Read Larry Desjardin's "Outside the Box" blog at www.tmworld.com/blogs.

Let's get small!

One of the advantages of modular instrumentation is its reduced size compared to traditional equipment. Eliminate the keyboards and displays and do more via virtual instrumentation, and you can easily achieve five-to-one size savings or even more. At one time, this wasn't considered such a big deal, but more and more applications are seeing real benefits from down-sized instrumentation. Here's why:

• *Size is sometimes mission-critical.* Small size is essential for many military test systems. Deploying a squadron of jet fighters in the desert involves more than just moving pilots and airplanes to a new location; there is a big logistics tail that needs to be deployed as well, including spare parts and test equipment. Years ago, large rack-and-stack ATE (automated test equipment) systems threatened to take more space than the weapon systems they were made to support. Imagine multiple C-130 cargo planes full of big, heavy test equipment, and you can imagine the problem. This is when military programs such as MATE, IFTE, and CASS mandated modular down-sized equipment. It was this imperative that led to the creation of the VXIbus, the first open modular architecture.

What's worse than deploying equipment in the desert? How about storing equipment on an aircraft carrier! Ships have extremely limited space, and they are meant to store crew, planes, and ordnance, not to be filled up by bulky test equipment. This is why when it comes to defense, small size is often mission-critical.

• *Small size offers cost advantages to commercial manufacturing.* Factory footprint costs money: lease costs, utility costs, HVAC, etc. Keeping test stations to a single rack minimizes needed rack space, while cabling and fixturing also become less expensive as size is reduced. Logistics become easier, too. Small size gives flexibility in integrating with the rest of a manufacturing line.

Small size means the spares are small, too. A 24×7 factory must be able to swap instruments quickly. Small size means small storage space for critical spares.

• *Small size is now delivering higher performance.* Two trends are having a significant effect on fixturing: higher-frequency RF applications and higher-speed digital buses. These higher speeds need shorter-length cabling to the DUT (device under test), which is easier to accomplish when the instrumentation ports are geographically concentrated. In this case, down-sized instruments come to the rescue again.

Think of it this way: If you have to cable from the DUT to test equipment along the entire height of a rack, the cable lengths can be up to half the rack height. The more you can concentrate high-frequency instrumentation densely to the center of the rack, the shorter those spans. You'll experience less signal loss, require less calibration, and obtain higher-fidelity signals at the other end.

But why does "small" often mean "modular"? Modular instrumentation enables a smaller footprint in three ways:

• *Modular instruments are inherently smaller.* By eliminating front panels, keyboards, and redundant power supplies, modular instruments take a fraction of the rack space of traditional instruments.

• *Modular instruments often take advantage of virtual instrumentation.* Powerful software can make many measurements mathematically from a single ADC and front end. This eliminates redundant instruments types. While this concept can also be deployed for traditional instruments, it isn't as common. Because modular instruments have the software disaggregated from the hardware, virtual instrumentation is a more natural fit with modular instruments.

• *Modular instruments are faster.* Faster systems mean you need fewer systems in a manufacturing environment, which directly reduces floor space and cost.

Small, fast, flexible. All delivered on modern modular platforms. So, the next time you are thinking of a big idea for test strategy, think small. T&MW

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